

DESIGN OF 2.4 GHz CMOS POWER AMPLIFIER FOR WIRELESS COMMUNICATION

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ABSTRACT

This paper gives the information about designing the 2.4GHz CMOS power amplifier for wireless communication using 130nm technology. Previously work present different approaches for designing the CMOS power amplifier for different class with different technology. This paper proposed class-B power amplifier using 130 nm technology for gain more than 15dB. The class-B power amplifier is design and to meet the frequency response for 2.4 GHz with gain of 67.321dB, the proposed power supply work with the voltage from 1.3 to 3V, which means that we can used these design for battery aided hand held electronic moving or electronic mobile communication equipment .The proposed power amplifier is designed using ADS tool.

Keyword: Gain, CMOS devices, radio frequency, design under test, error vector magnitude.

I. INTRODUCTION

This research deals with Power Amplifiers is part of the transmitter front-end, and are used to amplify the signal being transmitted so that it can be received and decoded within a fixed geographical area. The research in the area of power amplifiers is divided into two main categories; the design and monolithic implementation of power amplifiers, and the integration of Linearization techniques.

The main performance parameters for the power amplifier are the level of output power it can achieve, depending on the targeted application, linearity, and efficiency. There are two basic definitions for the efficiency of the power amplifier. The drain efficiency is the ratio between the RF output power to the dc consumed power, and the power added efficiency (PAE) which is the ratio between the difference of the RF output power and the RF input power to the dc consumed power. The PAE is a more practical measure as it accounts for the power gain of the amplifier. The power gain of amplifier can be improved by increasing stages but by compromising power consumption as each stage will consume a certain amount of power, the overall power consumption will increase.

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II. RELATED STUDY

According to [1] describes Power amplifier is the key component in wireless trans receiver and its realization and integration in standard CMOS technology is essential for the efficient and cost effective wireless silicon on chip. In this work, present a fully integrated differential power amplifier operating at 2.45GHz realized in 0.18 μ m RF CMOS process. The designed power amplifier has a built in capability to modulate the base band signal using On - Off Keying (OOK) while providing a single ended output power of over +6.4 dBm to 50 Ω load impedance.

According to [2] describes A fully integrated 2.4GHz power amplifier with high output power in standard 0.18 μ m CMOS process for WIMAX application is presented for increasing linearity and efficiency, a parallel cascade class A&B power amplifier is used. The proposed work in the paper with 3.3v power supply provides maximum output power of 32.5 dBm and power added efficiency 37.9% at 2.4 GHz operating frequency.

According to [3] describes Power Amplifier is an essential part of wireless power transfer system. To comprehensively investigate the wireless power transfer using mid-range resonant coupling over a wide range of frequencies, the analysis and design of a RF power amplifier covering a broadband of 2-30MHz are presented. The power amplifier works in class AB mode to achieve both the high efficiency and high rated output power. The amplifier features a configuration of multilayer media. In this aspect, method of moment (MOM) is employed to analyze the amplifier for its exclusive advantage in modelling

multilayer medium problems. A prototype amplifier, operating at an output power of more than 50 W with PAE of more than 45% over the frequency band of 2-20 MHz.

According to [4] describes a novel bipolar-MOSFET (BiFET) cascade differential power amplifier (PA) is proposed and fabricated, showing strong improvement on the linearity performances over those of the conventional bipolar-bipolar cascade PA. The two-stage differential BiFET cascade PA achieves Pout of 25.7 dBm with 52.1% power added- efficiency (PAE) in the continuous wave measurement at 900 MHz. A conventional bipolar-bipolar cascade PA is designed in a similar configuration to compare with the BiFET cascade PA performances. Power amplifier in terms of error vector magnitude (EVM), adjacent channel leakage ratio (ACLR) and the transmission output spectra. These linearity improvements are more visible at lower Pout levels, and become particularly striking as the signal bandwidth increases to 20 MHz. The SiGe PAs are designed and fabricated in a 0.35- μm SiGe BiCMOS technology with through-wafer-vias (TWVs) for low-power broadband wireless applications.

In the earlier approaches mainly problem with the size of chip, gain and frequency, which is overcome by 130nm technology due to this size is reduce with maintained frequency range and improved gain of COMS power amplifier.

III. RESEARCH METHODOLOGY TO BE EMPLOYED

STEP 1:- Selection of MOS Device

This is the first and the most important step while designing an on chip power amplifier . The selection of MOS depends on its mobility, so we have selected an enhancement type of n-MOS transistor. The three important parameters in the transistor are V_{ds} , V_{gs} and I_{ds} . Values of V_{ds} and V_{gs} are predetermined. We have to obtain the desired value of I_{ds} which is dependent on W/L ratio of MOS transistor. The only parameter on which the I_{ds} depends is "width" of the device.

$$I_{ds} = (\mu_n * C_{ox} / 2) * (W/L) * (V_{gs} - V_t)^2$$

Values of μ_n and C_{ox} are dependent on fabrication process.. For simulation purpose we are using BSIM 3 model, hence the device width is reduced by 20% to 30% of the calculated width.

STEP 2:- DC Simulation

The importance of DC simulation is to determine the quiescent point of the device MOS. The DC Simulation controller calculates the DC operating characteristics of a design under test (DUT). Fundamental to all RF/Analog simulations, DC analysis is used on all RF/Analog designs. It

performs a topology check and an analysis of the DC operating point, including the circuit's power consumption. The simulator computes the response of a circuit to a particular stimulus by formulating a system of circuit equations and then solving them numerically. The DC simulation accomplishes this analysis as follows:

- Solves a system of nonlinear ordinary differential equations (ODEs)
- Solves for an equilibrium point
- All time-derivatives are constant (zero)
- System of nonlinear algebraic equations

We can also set up the DC simulation to sweep one or more parameters, enabling you to perform tasks such as verifying model parameters by comparing the simulated DC transfer characteristics (I-V curves) of the model with actual measurements. We are using a fixed biasing scheme for DC biasing. In self bias and voltage divider bias, resistors are involved, which increase the size and parasitic effect of device. So we are using self bias to optimize the device.

Biasing in electronics is the method of establishing predetermined voltages or currents at various points of an electronic circuit to set an appropriate operating point. The operating point of a device, also known as bias point, quiescent point, or Q-point, is the steady-state operating condition of an active device (a transistor or vacuum tube) with no input signal applied.

STEP 3:- Feedback Network Design

Feedback can be either negative or positive. In amplifier design, negative feedback is applied to effect the following properties.

1. Desensitize the gain
2. Reduce non-linear distortion
3. Reduce the effect of noise
4. Control the input and output impedance

Feedback can be classified into four categories as given below,

1. Series-shunt feedback (Voltage Amplifier)
2. Shunt-series feedback (Current Amplifier)
3. Series-series feedback (Transconductance Amplifier)
4. Shunt-shunt feedback (Transresistance Amplifier)

STEP 4:- S Parameter Analysis

Scattering parameters are all about power, both reflected and incident in a linear two port system. It assumes that the system must be treated like a transmission line system; lumped elements no longer adequately describe the system. For the following analysis, refer to Figure 1.

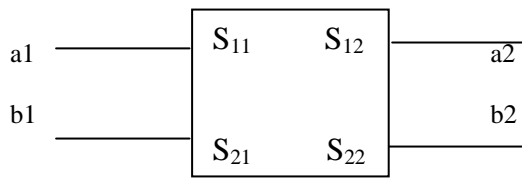


Figure1: S Parameter Two Port Model

The s-parameter definition is:

$$b_1 = a_1 S_{11} + a_2 S_{12}$$

$$b_2 = a_1 S_{21} + a_2 S_{22}$$

where,

$$|a_1|^2 = \text{Power incident on the input of the network.}$$

$$= \text{Power available from source impedance } Z_0.$$

$$|a_2|^2 = \text{Power incident on the output of the network.}$$

$$= \text{Power reflected from the load.}$$

$$|b_1|^2 = \text{Power reflected from input port of network.}$$

$$|b_2|^2 = \text{Power reflected from the output port of the network.}$$

$$= \text{Power incident on the load.}$$

$$= \text{Power that would be}$$

$$\text{delivered to a } Z_0 \text{ load.}$$

And

$$|S_{22}| = \frac{\text{Power reflected from the network output}}{\text{Power incident on the network output}}$$

$$|S_{21}| = \frac{\text{Power delivered to } Z_0 \text{ load}}{\text{Power available from } Z_0 \text{ source}}$$

= Transducer power gain with both load and source having impedance as Z_0 .

$|S_{12}|$ = Reverse Transducer power gain with Z_0 load and source.

STEP 5:- Noise Figure Analysis

Besides stability and gain, another important design consideration for a microwave amplifier is its noise figure. In receiver applications, it is often required to have a preamplifier with as low a noise figure as possible, as the first stage of a receiver front end has the dominant effect on the noise performance of the overall system. The noise figure parameter, N , are given where, the quantities F_{min} , Γ_{opt} and R_N are the characteristics of the transistor being used and are called the noise parameters of the device. It is the ratio of output SNR to input SNR in dB.

$$NF(dB) = 10 \log \frac{SNR_o}{SNR_i}$$

STEP 6:- Impedance Matching

The impedance matching network is lossless and is placed between the input source and the device. The need for matching network arises because amplifiers, in order to deliver maximum power to a load, or to perform in a certain desired way must be properly terminated at both the input and the output ports. The impedance matching networks can be either designed mathematically or graphically with the aid of Smith Chart. Several types of matching networks are available, but the one used in this design is open single stubs whose length is found by matching done using smith chart manual.

In RF circuits, we very seldom start with the impedance that we would like. Therefore, we need to develop techniques for transforming arbitrary impedance into the impedance of choice. For example, consider any RF system. Here the source and load are 50V (popular impedance), as are the transmission lines leading up to the IC. For optimum power transfer, prevention of ringing and radiation, and good noise behaviour, for example, we need the circuit input and output impedances matched to the system. In general, some matching circuit must almost always be added to the circuit. Typically, reactive matching circuits are used because they are lossless and because they do not add noise to the circuit. However, using reactive matching components means that the circuit will only be matched over a range of frequencies and not at others. If a broadband match is required, then other techniques may need to be used. The series inductance adds impedance of $j\omega L$ to cancel the input capacitive impedance. Note that, in general, when an impedance is complex ($R + jX$), then to match it, the impedance must be driven from its complex conjugate ($R - jX$).

IV. BLOCK DIAGRAM

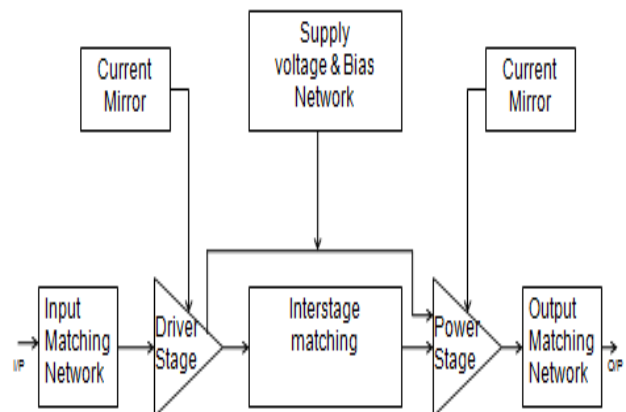


Figure 2: Block Diagram

The fig.2 shows the functional block diagram of the Power Amplifier. Input matching and Output matching networks are used at input and

output stage respectively to minimize return losses. Input matching is done by calculation of input impedance using the ratio of the input voltage and input current. The magnitude of the input reflection ratio is calculated using the input impedance of the amplifier, and used to derive the value of S_{11} . The same concept is utilized to find S_{22} . A inter stage matching network is also used as multiple stages will be used for power amplification.

Driver stage and Power stage with the supply bias network are main blocks of the power amplifier. Current mirror is used for the biasing of the circuit.

V. CALCULATION OF POWER GAIN

Power amplifiers are required to boost the transmitted signal by providing a signal gain to the output of the preceding stage, usually a mixer. Power/Voltage gain is the ratio of output power/voltage (delivered to the load) to the input power/voltage. The power gain will be equal to the voltage gain of the amplifier only if the input and output impedances are the same.

Fig.3 shows circuit diagram for calculating the power gain for calculating the power gain the required input for circuit is set as per the requirement in the circuit, the frequency is set to be in the range of 2-3GHz,in input T filter network the capacitor is set to 218.267fF,inductor is set to 12.911nH and resistor is set to as 1Kohm.The input impedance is set as 50ohm.In the output circuit the value of required circuit is tunned as per the requirement to calculate the range of power gain.

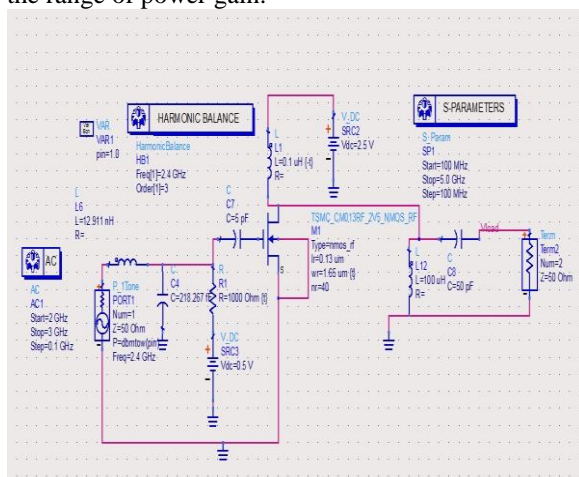


Figure 3: circuit diagram for power gain

The fig.4 shows the output graph of power gain. The graph is power input gain as shown in graph. On x axis 1div equal to 10,on y axis 1div equal to 2dB.The achieved maximum gain ie.m5 is 36.109dB at -50 input power where as minimum gain i.e. m6 is obtained 35.206dB when input power is -26.300.

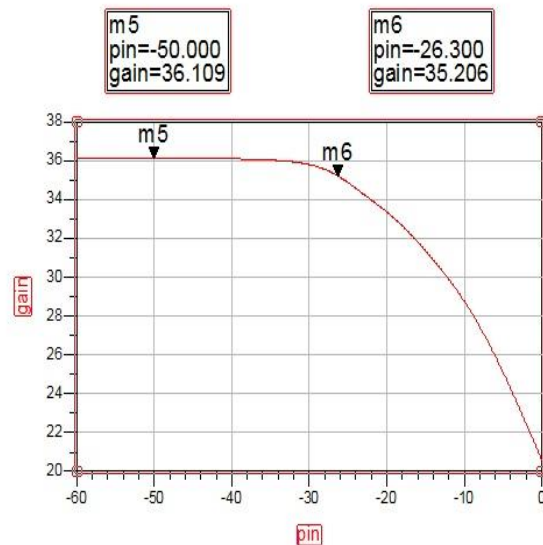


Figure 4:Output for power gain

Fig.5 shows output of class-B amplifier for power gain. The graph shows frequency verses gain, on x-axis 1div equal to 0.5 Hz, and on y-axis 20dB.The achieved gain ie.m3 is 67.321dB at 2.4GHz.The maximum gain is achieved at 2.4GHz ie.67.321dB.

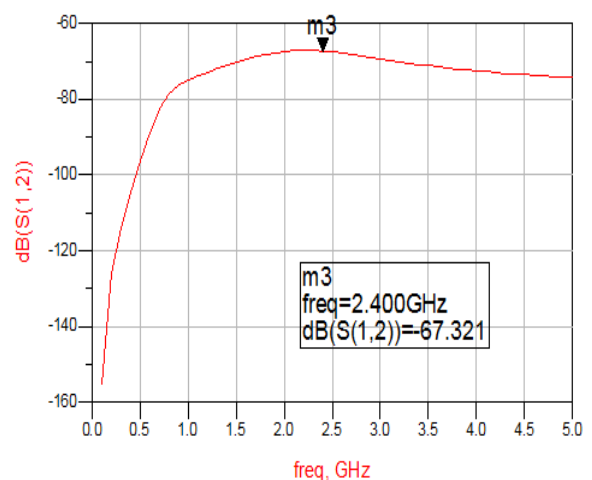


Figure 5: Output of class-B amplifier for power gain

VI. CONCLUSION

The project “Design of 2.4GHz CMOS power amplifier for wireless communication” has been successfully designed. Implementing power amplifiers in CMOS technology is considered a major step towards the realization of a complete transceiver on-chip. Modern transceivers require means for adjusting the transmitted power over a finite range to further reduce power consumption and improve channel capacity. A high level of integration, and low cost can be achieved using CMOS technology.

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